Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A digital signal processor comprising:

two execution pipelines capable of executing RISC and DSP instructions;

instruction fetch logic that simultaneously fetches two instructions and routes them to respective pipelines; and

control logic to allow the pipelines to operate independently.

2. (Original) The digital signal processor of claim 1, wherein the instruction fetch logic includes logic that fetches dual SIMD instructions.

3. (Original) The digital signal processor of claim 1, further including two registers each half the length of a word fetched for memory, and

wherein the instruction fetch logic fetches a single word into the two registers simultaneously.

4. (Original) The digital signal processor of claim 1, further including an eight port general register file.

5. (Original) The digital signal processor of claim 4, wherein the general register file includes four read registers and four write registers.

6-10. (Cancelled).

11. (New) The digital signal processor of claim 1 wherein each of the two execution pipelines is capable of executing both RISC and DSP instructions.

12. (New) The digital signal processor of claim 1 wherein one of the execution pipelines is dedicated to processing RISC instructions and one of the execution pipelines is dedicated to processing DSP instructions.

13. (New) A method for processing instructions in a digital signal processor, the method comprising:

simultaneously fetching a first instruction and a second instruction;

routing the first instruction to a first execution pipeline and the second instruction to a second execution pipeline, wherein the first execution pipeline and the second execution pipeline are capable of executing RISC and DSP instructions; and

using control logic to operate the first execution pipeline and the second execution pipeline independently.

14. (New) The method as in claim 13 wherein simultaneously fetching the first instruction and the second instruction includes simultaneously fetching dual SIMD instructions.

15. (New) The method as in claim 13 further comprising simultaneously fetching a single word into a first register and a second register, wherein the first register and the second register are each half a length of a word.

16. (New) The method as in claim 13 wherein the first execution pipeline and the second execution pipeline are each capable of executing both RISC and DSP instructions.

17. (New) The method as in claim 13 wherein the first execution pipeline is dedicated to processing RISC instructions and the second execution pipeline is dedicated to processing DSP instructions.

18. (New) A system for processing instructions, comprising:

an instruction memory having instructions; and

a digital signal processor that includes:

two execution pipelines capable of executing RISC and DSP instructions;

instruction fetch logic that simultaneously fetches two instructions from the instruction memory and routes them to respective pipelines; and

control logic to allow the pipelines to operate independently.

19. (New) The system of claim 18 wherein the instruction fetch logic includes logic that fetches dual SIMD instructions.

20. (New) The system of claim 18 further including two registers each half the length of a word fetched for memory, and

wherein the instruction fetch logic fetches a single word into the two registers simultaneously.

21. (New) The system of claim 18 further including an eight port general register file.

22. (New) The system of claim 21 wherein the general register file includes four read registers and four write registers.

23. (New) The system of claim 18 wherein each of the two execution pipelines is capable of executing both RISC and DSP instructions.

24. (New) The system of claim 18 wherein one of the execution pipelines is dedicated to processing RISC instructions and one of the execution pipelines is dedicated to processing DSP instructions.